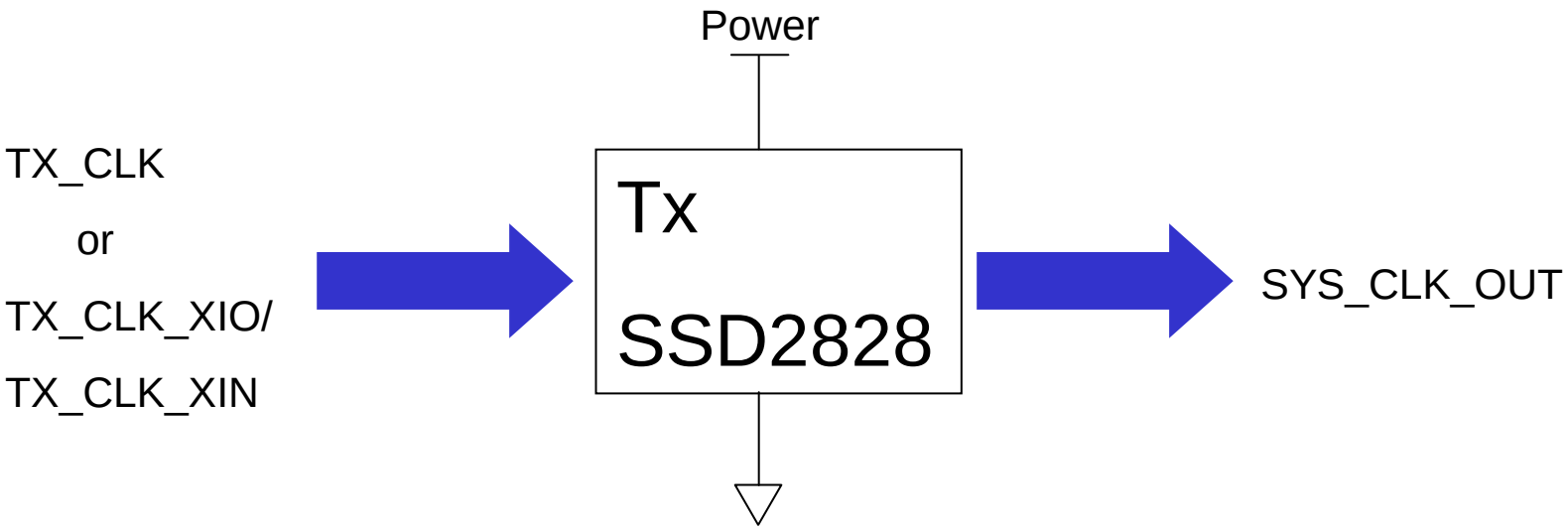
SSD2828 Debug Step

Guide Line

SSD2828 Debug Step 1

- Check SYS_CLK_OUT
  - No command and No RGB signals are needed
  - Power is supplied and TEST0 pin is properly connected
  - External CLK input (TX_CLK or TX_CLK_XIO/TX_CLK_XIN)
  - SYS_CLK_OUT can output same frequency of the external CLK



- Power, TEST0 and external CLK can be confirmed normal

SSD2828 Debug Step 2

- Check SPI write and read back
  - SPI pins are properly connected
  - SPI write for 0xB0 register read back request
  - ID 0x2828 can be read from SDO

3wire 24bit SPI read request

0x7000B0

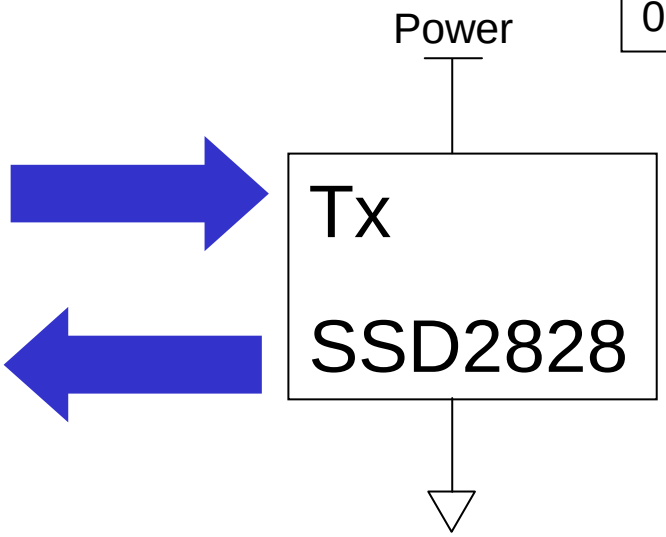
0x730000 Monitor SDO

SPI write:

0xB0 read back request

SPI read:

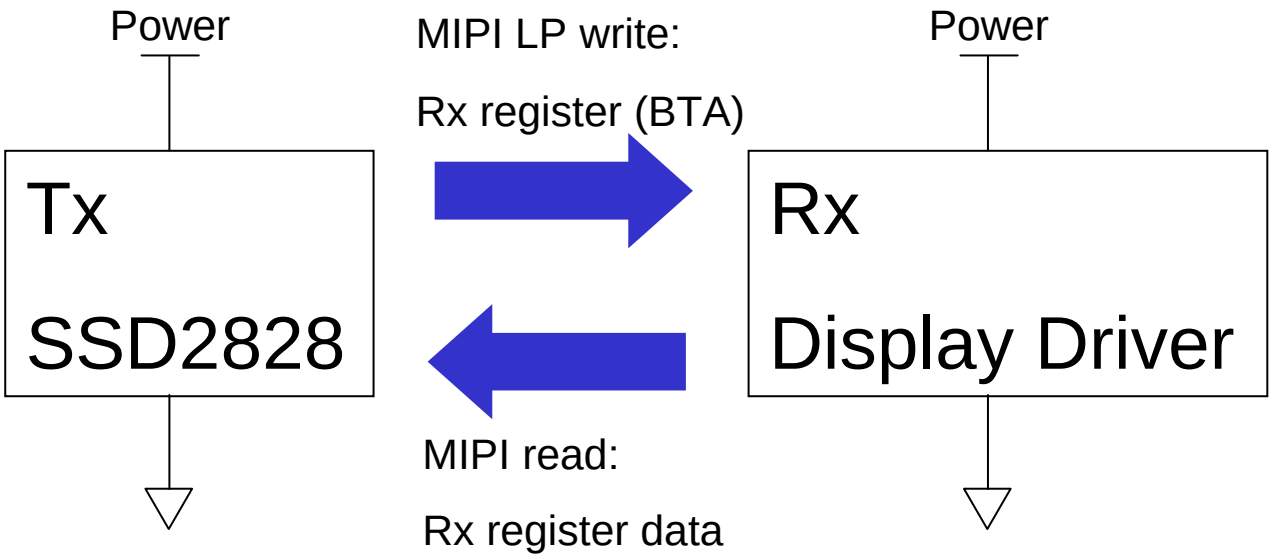
0x2828 ID is read



- SPI pins and SDO can be confirmed normal
- SPI logic can be confirmed normal

SSD2828 Debug Step 3

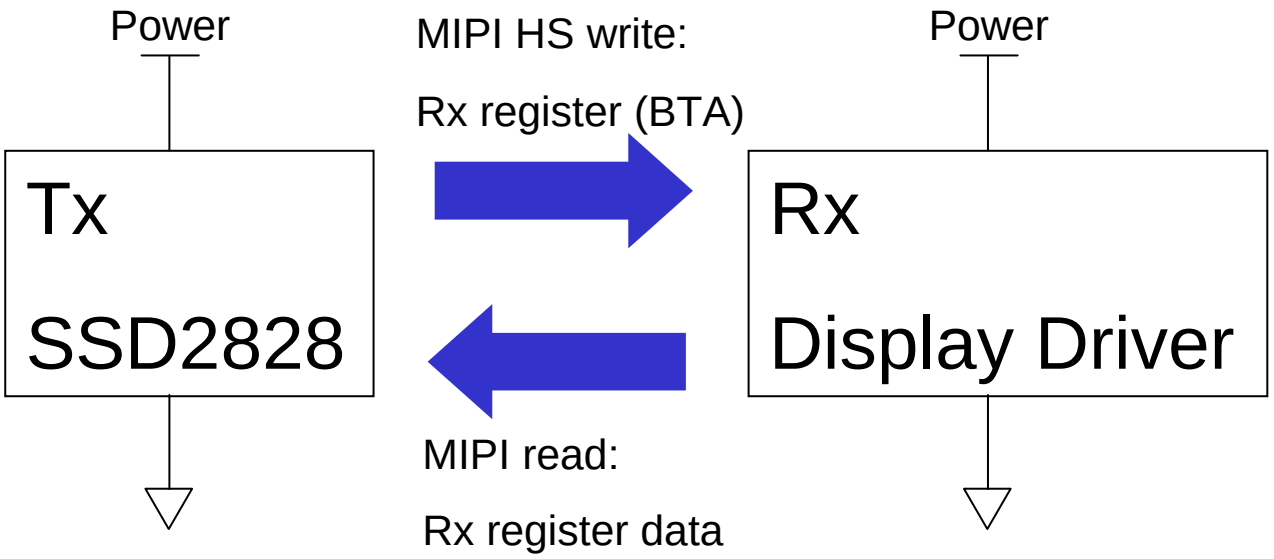
- Check MIPI LP write and read back
  - DP0 and DN0 pins are properly connected
  - MIPI LP write for Rx register read back request (BTA)
  - Rx register data can be read from DP0 and DN0



- DP0 and DN0 can be confirmed normal
- LP communication can be confirmed normal

SSD2828 Debug Step 4

- Check MIPI HS write and read back
  - MIPI data and clock pins are properly connected
  - MIPI HS write for Rx register read back request (BTA)
  - Rx register data can be read from DP0 and DN0

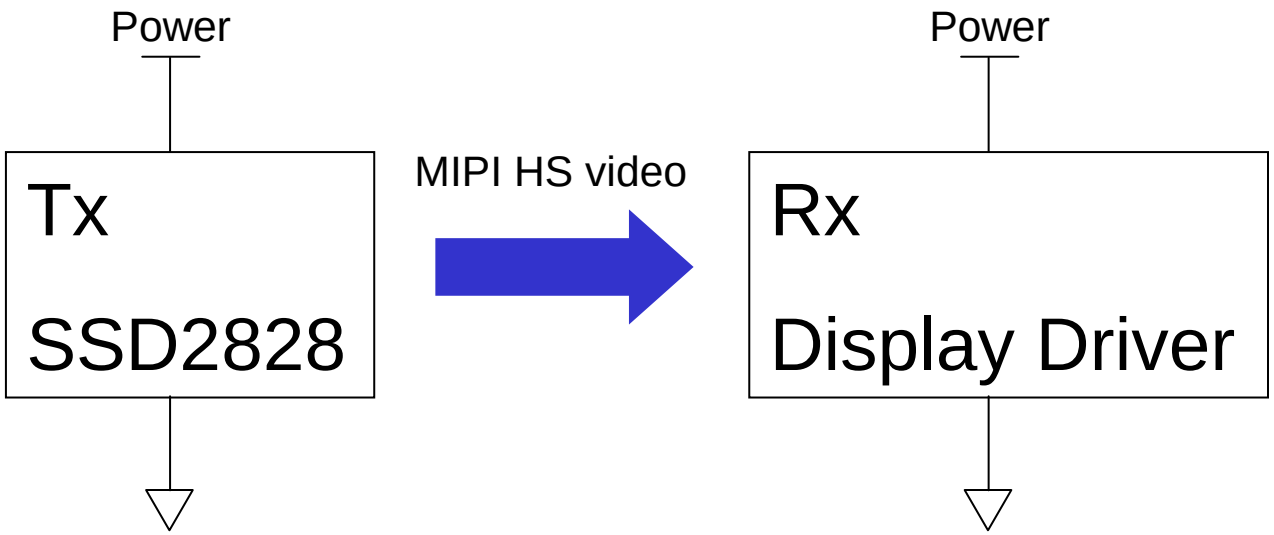


- MIPI data and clock pins can be confirmed normal
- HS communication can be confirmed normal

SSD2828 Debug Step 5 (Part 1)

Check MIPI HS video mode

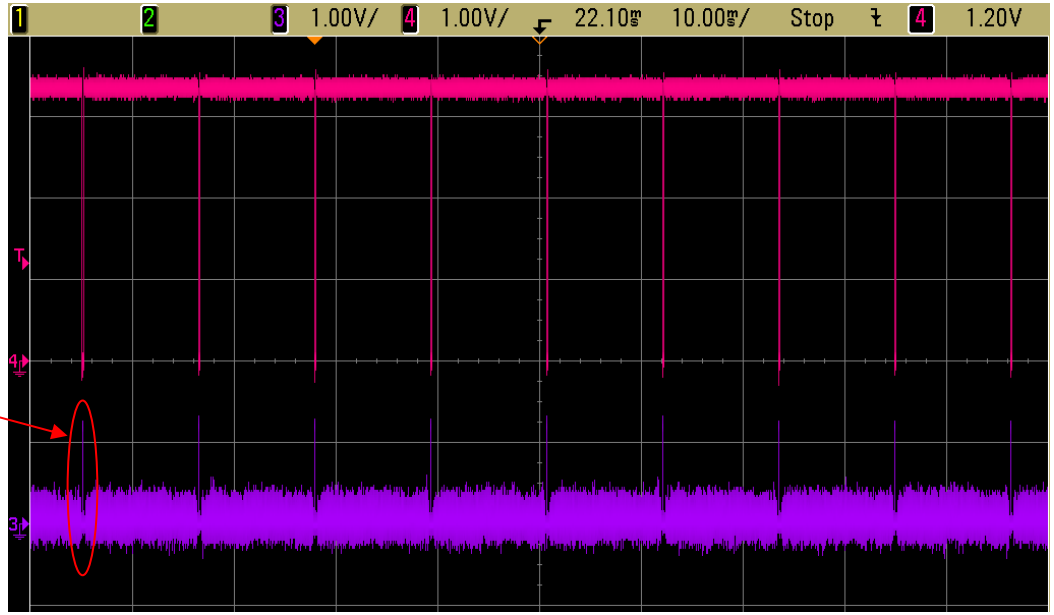
- RGB, MIPI data and clock pins are properly connected
- Blinking period (LP mode period) of the video mode must be synchronized with VSYNC signal



SSD2828 Debug Step 5 (Part 2)

Check MIPI HS video mode

- RGB, MIPI data and clock pins are properly connected
- Blinking period (LP mode period) of the video mode must be synchronized with VSYNC signal



Blinking period

(LP mode period)

- RGB, MIPI data and clock pins can be confirmed normal
- HS video can be confirmed normal

SSD2828 Read Diagram