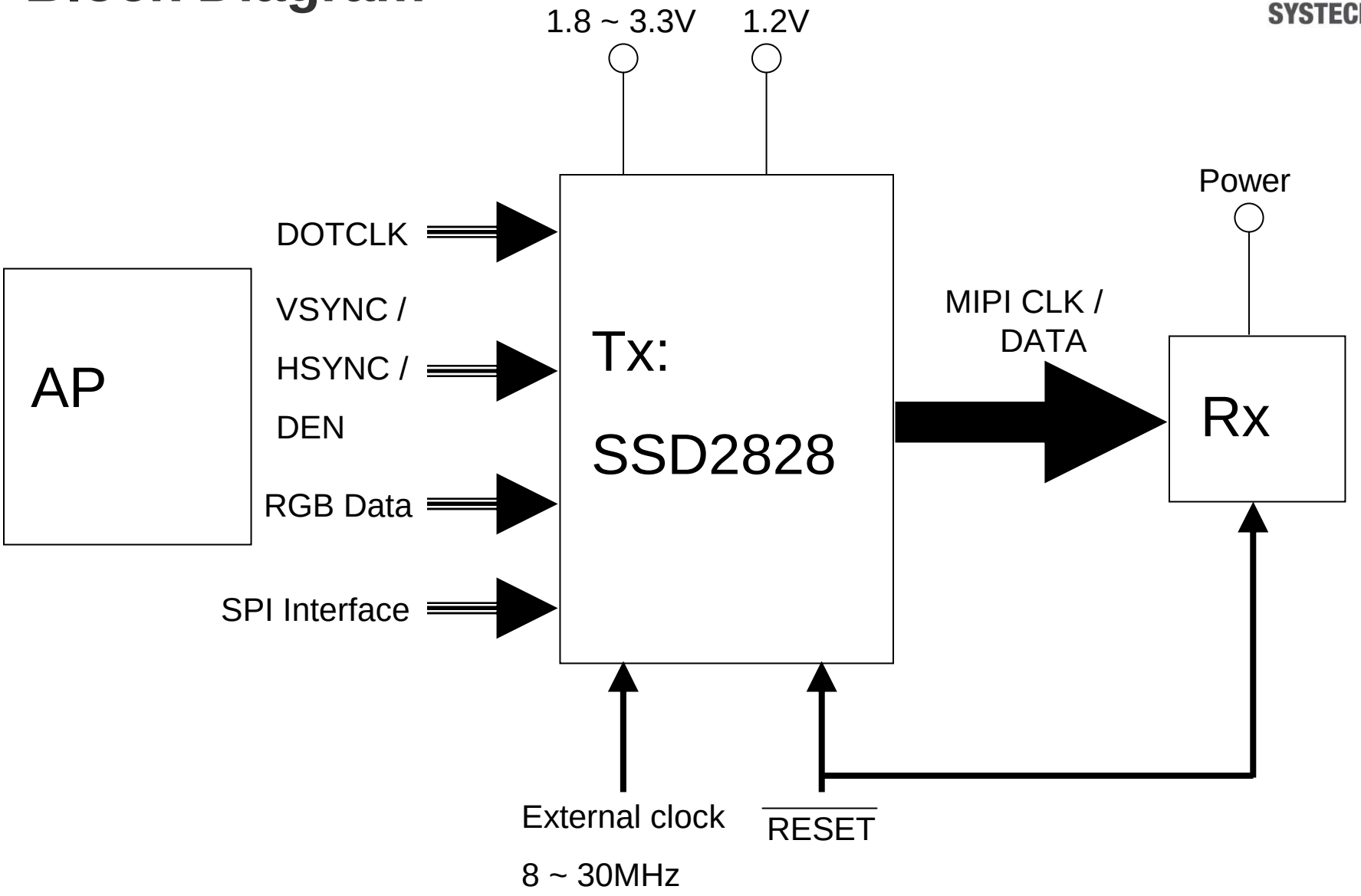
SSD2828 Getting Start User Guide

Version 02

Block Diagram



Check List

- 1. Hardware
  - A. Power Supply Voltage
  - B. External Clock Source
  - C. SPI Type
  - D. DOTCLK/HSYNC/VSYNC/DEN/RGB setting
  - E. Jumper setting

Check List

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  - E. VC setting for video and SPI mode
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Check List

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  - B. Video mode output

Check List

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  - A. No display, MIPI video cannot sync with VSYNC
  - B. No display, PLL > 600Mbps per lane
  - C. No display, even 0x11 and 0x29 are sent
  - D. End of the display has tearing effect
  - E. Display has red / blue / green dots
  - F. Display Shift

Check List

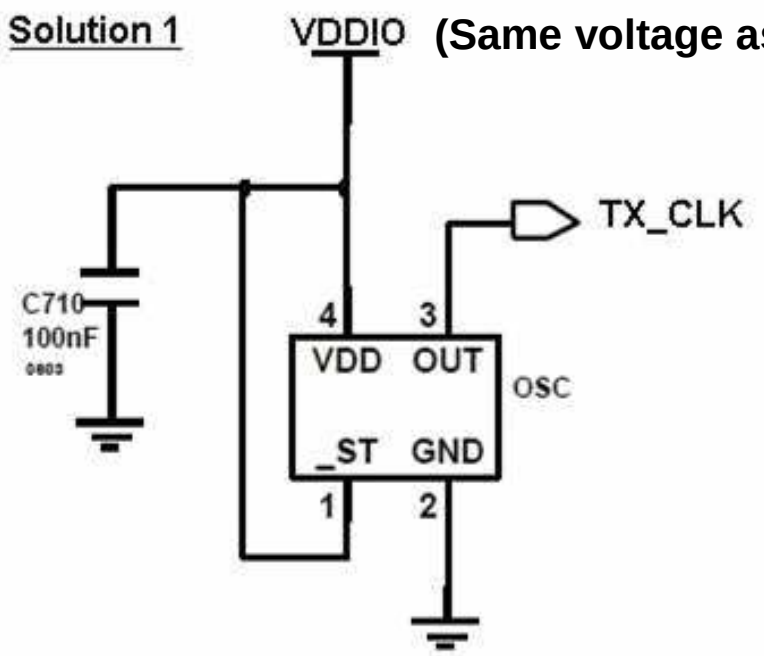
- 5. TS5000 debug guide
  - A. AP SYNC and RGB check

1A Power Supply Voltage

- MAVDD / MDVDD / VCC12A
  - Connected to 1.2V
  - Maximum current consumption is about 40mA
- VDD3IO / VDD3IOC / ATC[1:0]
  - Connected to 1.8 ~ 3.3V
  - Maximum current consumption is below 1mA

1B External Clock Source

- Setting of TEST[2:0] = **000**
- TX_CLK = 8 ~ 30MHz

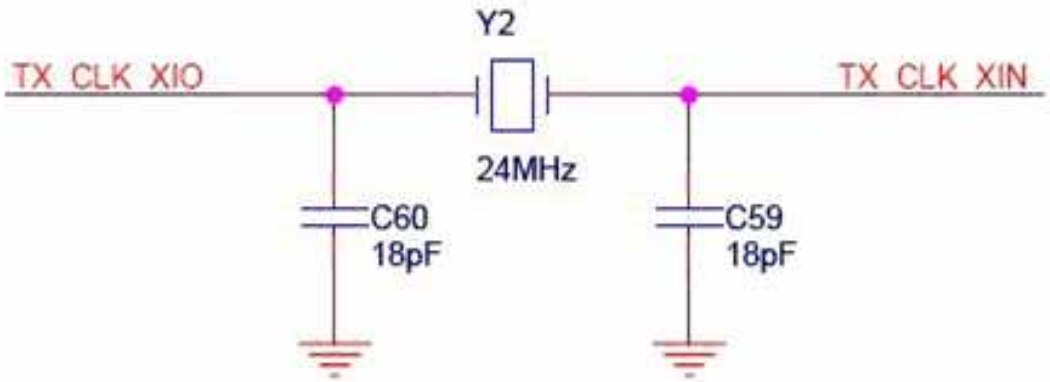


Pin	Connection
TX_CLK_XIN	VDDIO/GND
TX_CLK_XIO	VDDIO
TEST2	GND
TEST1	GND
TEST0	GND

1B External Clock Source

- Setting of TEST[2:0] = **001**
- Crystal freq. = 8 ~ 30MHz

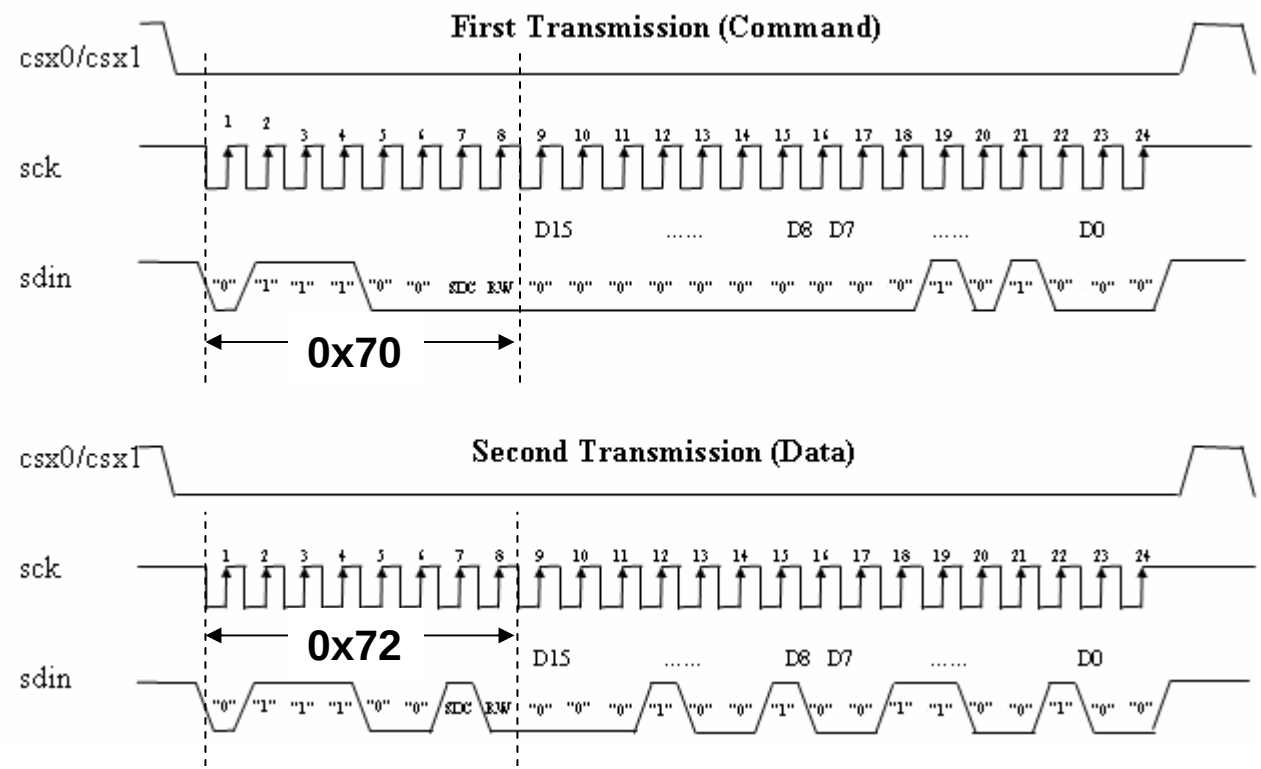
Solution 2



Pin	Connection
TX_CLK	VDDIO
TEST2	GND
TEST1	GND
TEST0	VDDIO

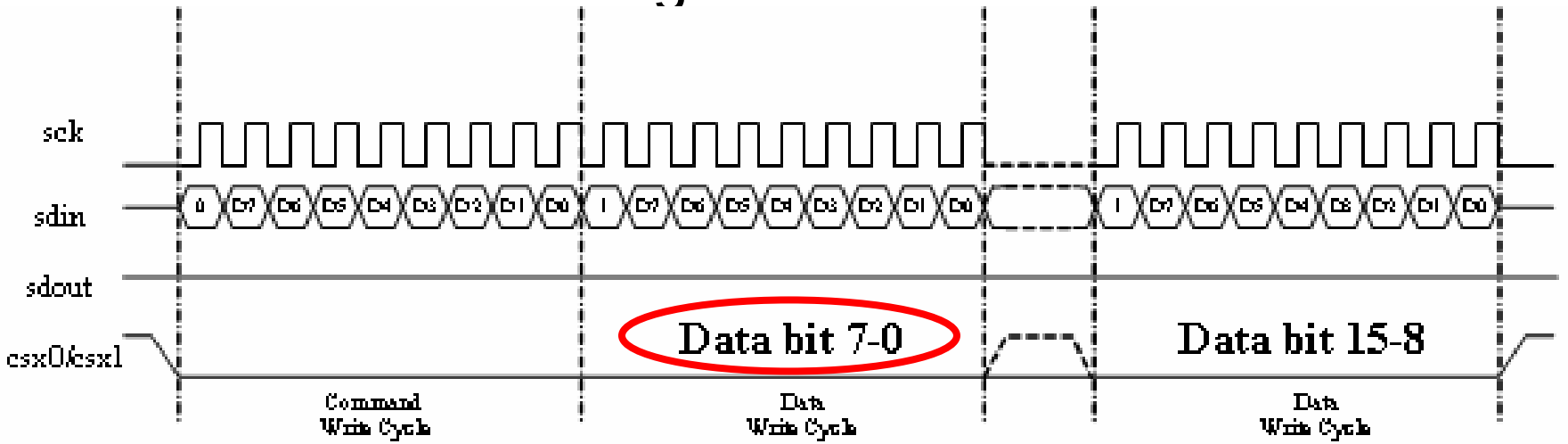
1C SPI Type

- PS[4:0] = 00000, 3 wire 24 bit SPI interface
- CSX0 is connected to CS pin of AP
- Make sure the MSB 8 bits are correct



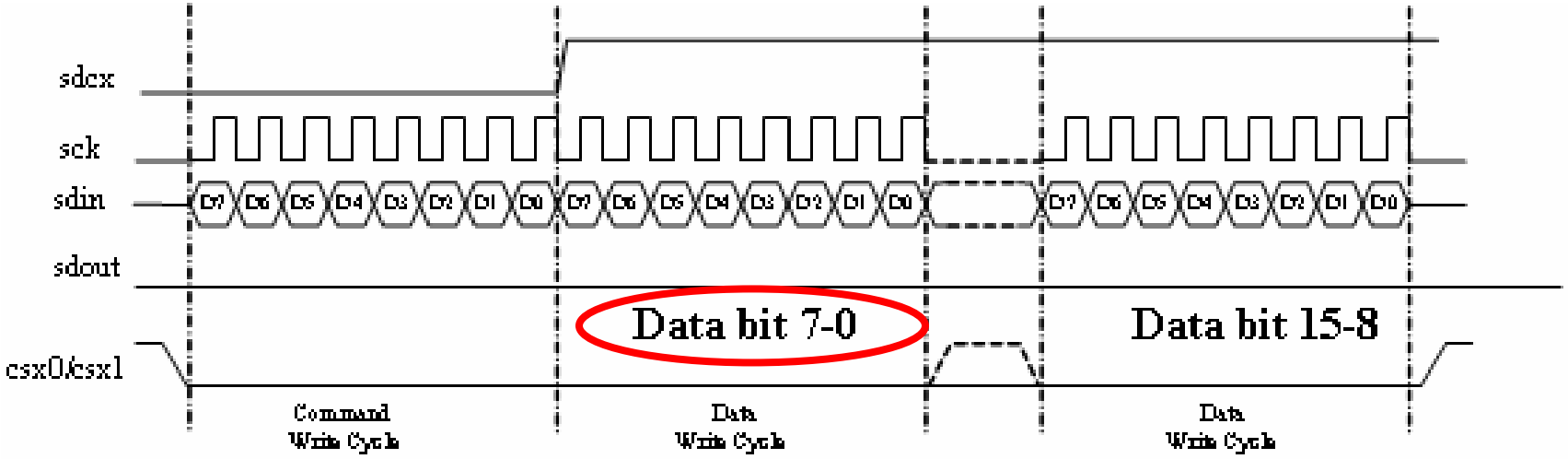
1C SPI Type

- PS[4:0] = 000001, 3 wire 8 bit SPI interface
- CSX0 is connected to CS pin of AP
- Make sure the MSB bit (D8) is “0” for command and “1” for data
- Make sure sending the LSB 8bit data first



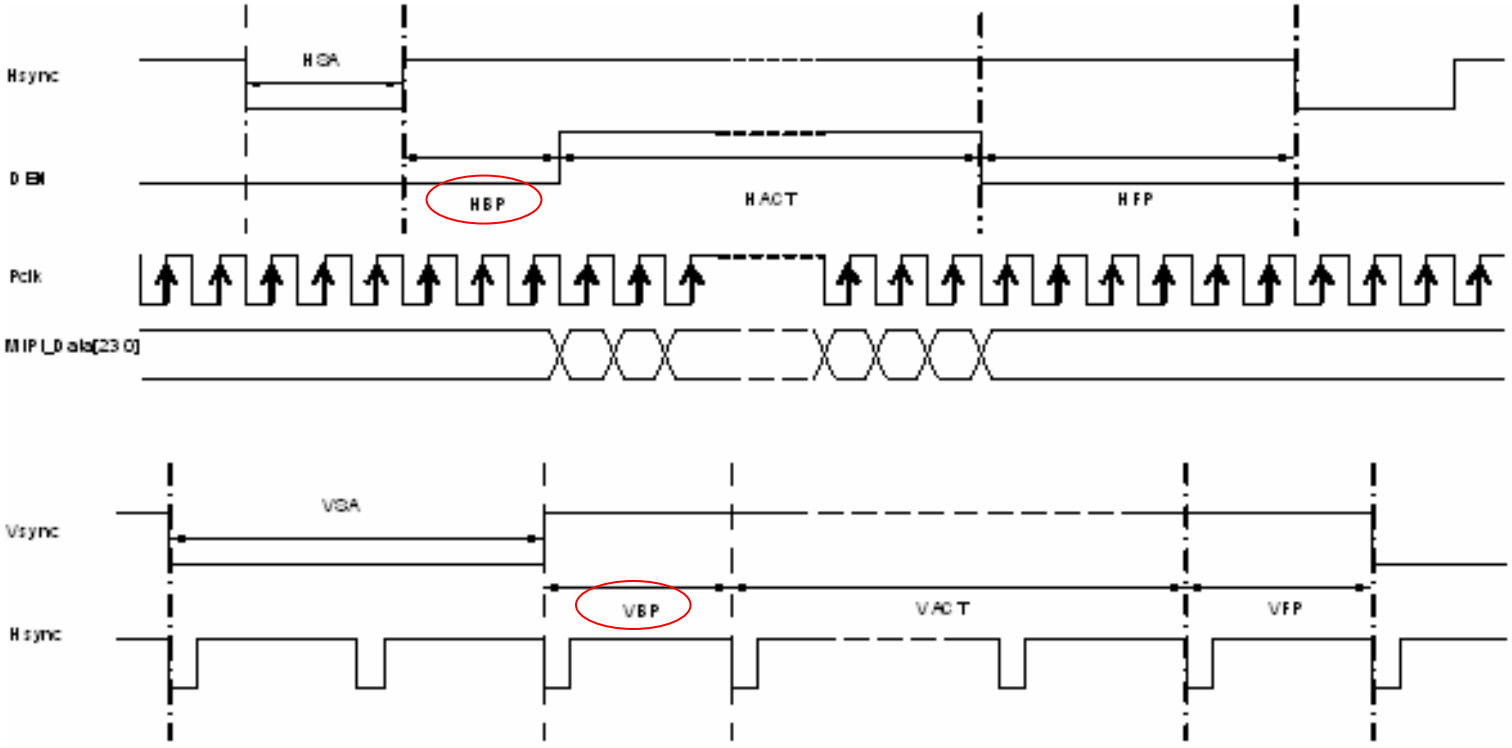
1C SPI Type

- PS[4:0] = 000010, 4 wire 8 bit SPI interface
- CSX0 is connected to CS pin of AP
- Make sure sending the LSB 8bit data first



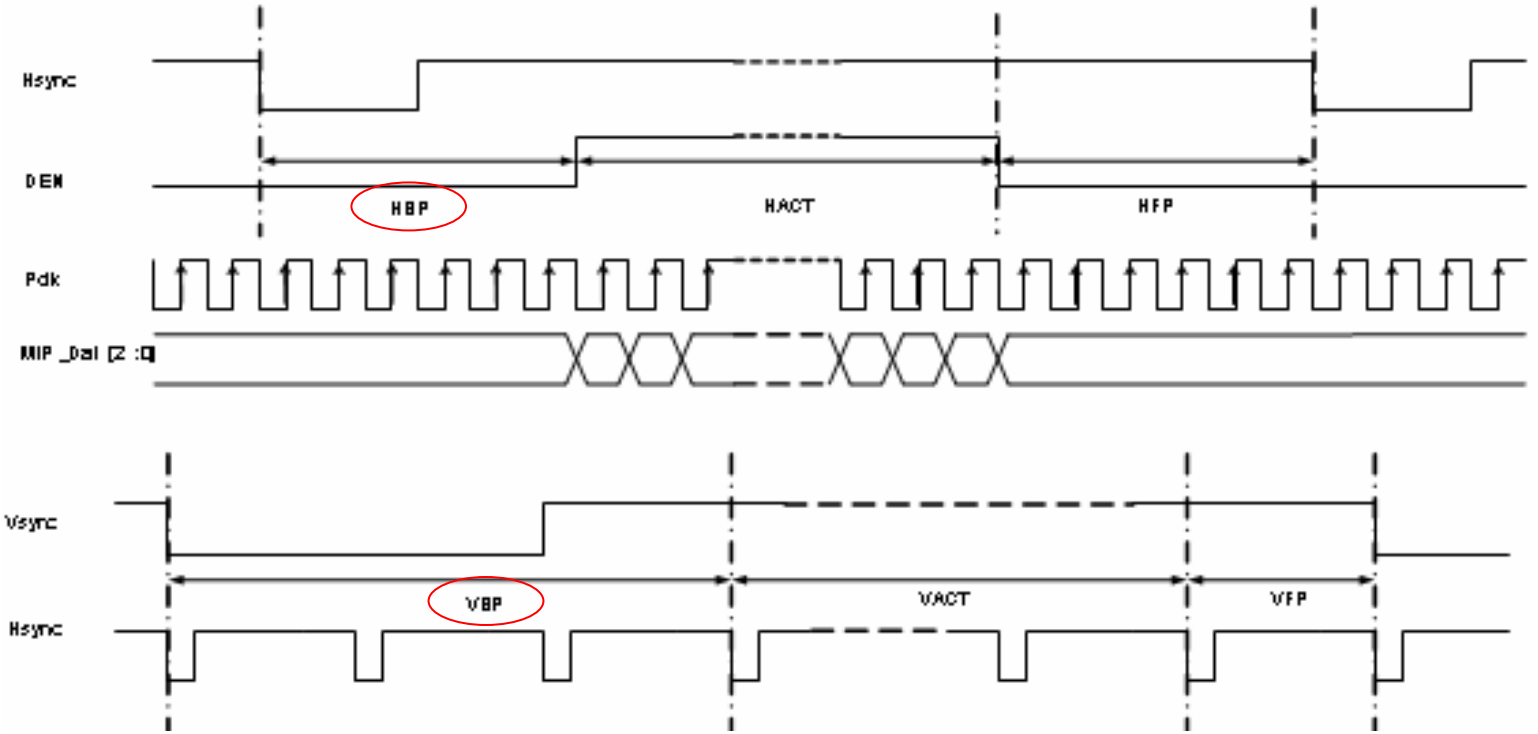
1D DOTCLK/HSYNC/VSYNC/DEN/RGB setting

- Sync Pulses event
- SYNC width will not be counted for back porch value



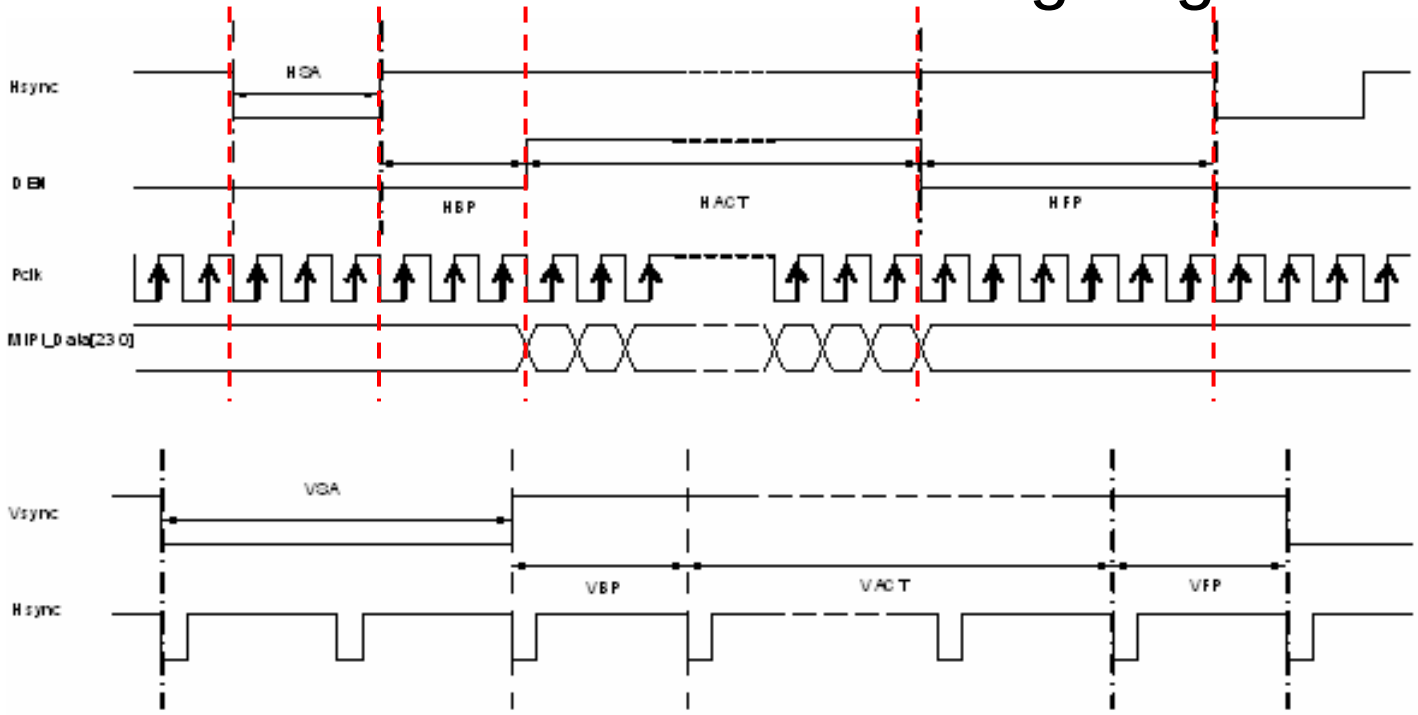
1D DOTCLK/HSYNC/VSYNC/DEN/RGB setting

- Sync event
- SYNC width will be counted for back porch value



1D DOTCLK/HSYNC/VSYNC/DEN/RGB setting

- Make sure PCLK is rising edge trigger
- Rising/Falling edge of HSYNC/VSYNC/DEN/DATA must be matched with PCLK falling edge



HSYNC is active low

DEN is active high

VSYNC is active low

1E Jumper setting

- CM = 0, 16M/262k/64k color display mode
- SHUT = 1, using software command to control display on/off
- IF_SEL = IF_SEL2 = 0, normal operation

2A HS clock setting (PLL clock)

- Minimum PLL clock frequency is related to PCLK
- E.g. PCLK = 55MHz, 24bit color, 4 Lanes
- Min. PLL freq. = 330Mbps

	PCLK	55.0	MHz
	Color	24	Bits
	# of Lane	4	
Min.	Per Lane Speed	330	Mbps

2A HS clock setting (PLL clock)

- Related commands:
  - 0xB9 Control PLL on/off
  - 0xBA PLL freq. setting
- PLL freq. can only be changed when PLL is off
- E.g. TX_CLK = 10MHz, 0xBA 0x8023
  - PLL = 350Mbps

2B LP clock setting

- Related commands:
  - 0xB9 Control PLL on/off
  - 0xBA PLL freq. setting
  - 0xBB LP clock setting
- E.g. TX_CLK = 10MHz, 0xBA 0x8023, 0xBB 0x000A
  - LP clock = 350Mbps / 10 / 8 / 2 = 2.2MHz

PLL freq. **0xBB 0x000A** **1 byte PLL generating 1 bit LP clock** **Convert unit "bps" to "Hz"**

2C DOTCLK/HSYNC/VSYNC/DEN setting

- Related commands:
  - 0xB1 SYNC width setting
  - 0xB2 Back porch setting
  - 0xB3 Front porch setting
  - 0xB4 Horizontal active period
  - 0xB5 Vertical active period
  - 0xB6 Video mode and pixel format
- Make sure all the settings are matched with AP, otherwise there is no display

2D Number of MIPI Lane setting

- Related command:
  - 0xDE Number of lane setting
- E.g. 0xDE 0x0000 = 1 Lane, 0xDE 0x0003 = 4 Lane

2E VC setting for video and SPI mode

- Related command:
  - 0xB8 Virtual Channel ID setting
- Normally, all the VC should be “00”, so 0xB8 0x0000 for most of the case

2F RGB Data setting

- Related command:
  - 0xD6 RGB or BGR setting
  - Following is an example:

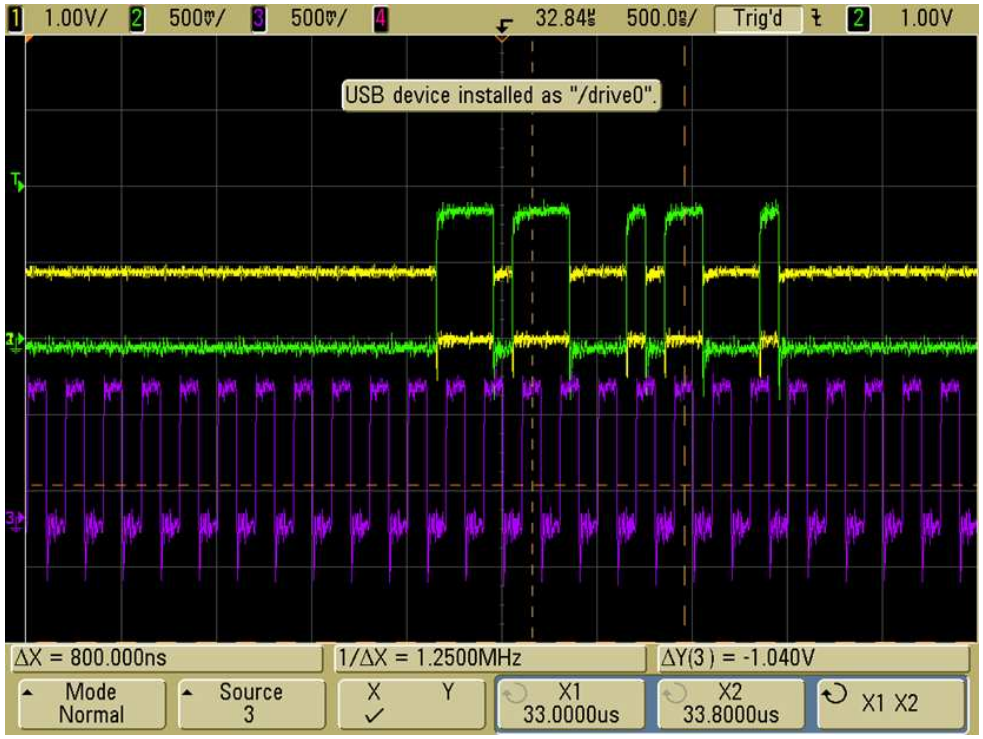
0xD6	CO	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x0004	**0**	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
0x0005	**1**	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0

  - 0xB6 24 / 18 / 16 bpp setting
  - Following is an example:

24bpp	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp	X	X	X	X	X	X	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp	X	X	X	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

3A HS mode MIPI connection

- If there is no MIPI connection with Rx
  - HS mode has about 1V peak to peak waveform



Legend

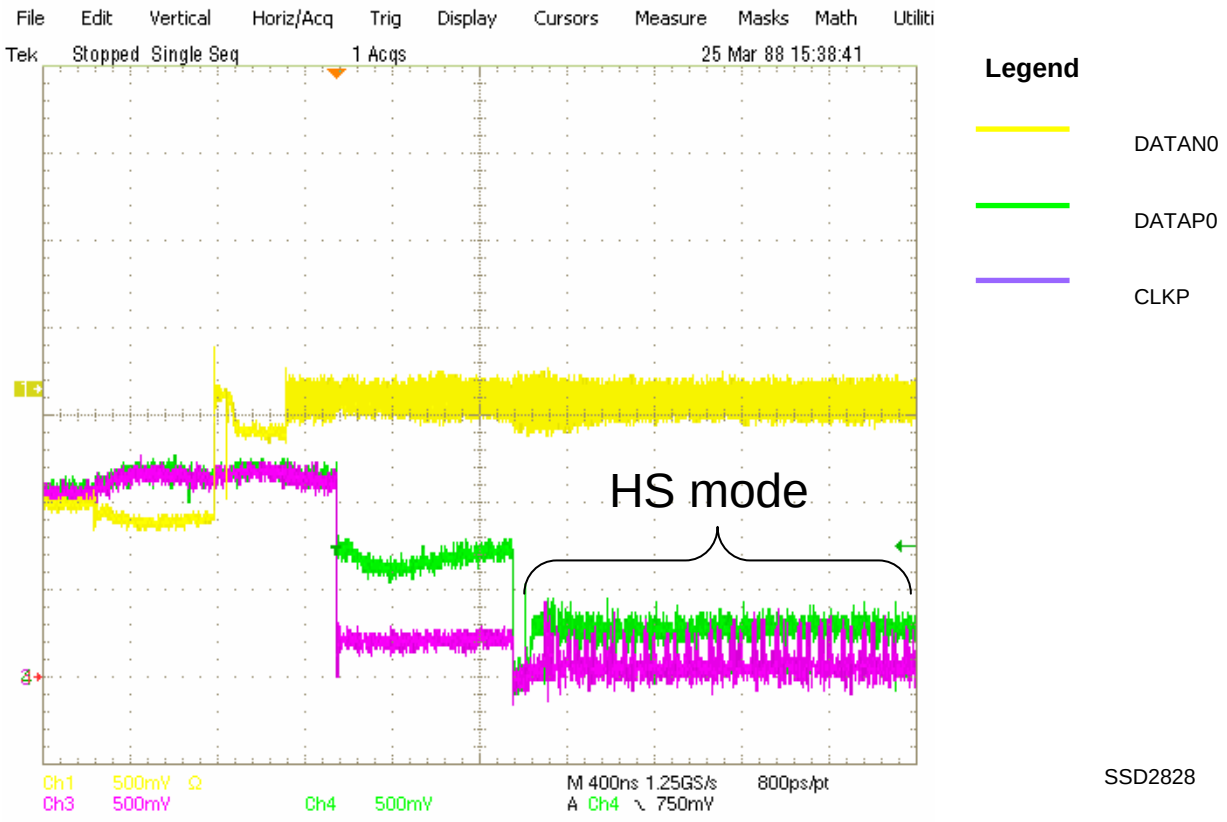
DATAN0

DATAP0

CLKP

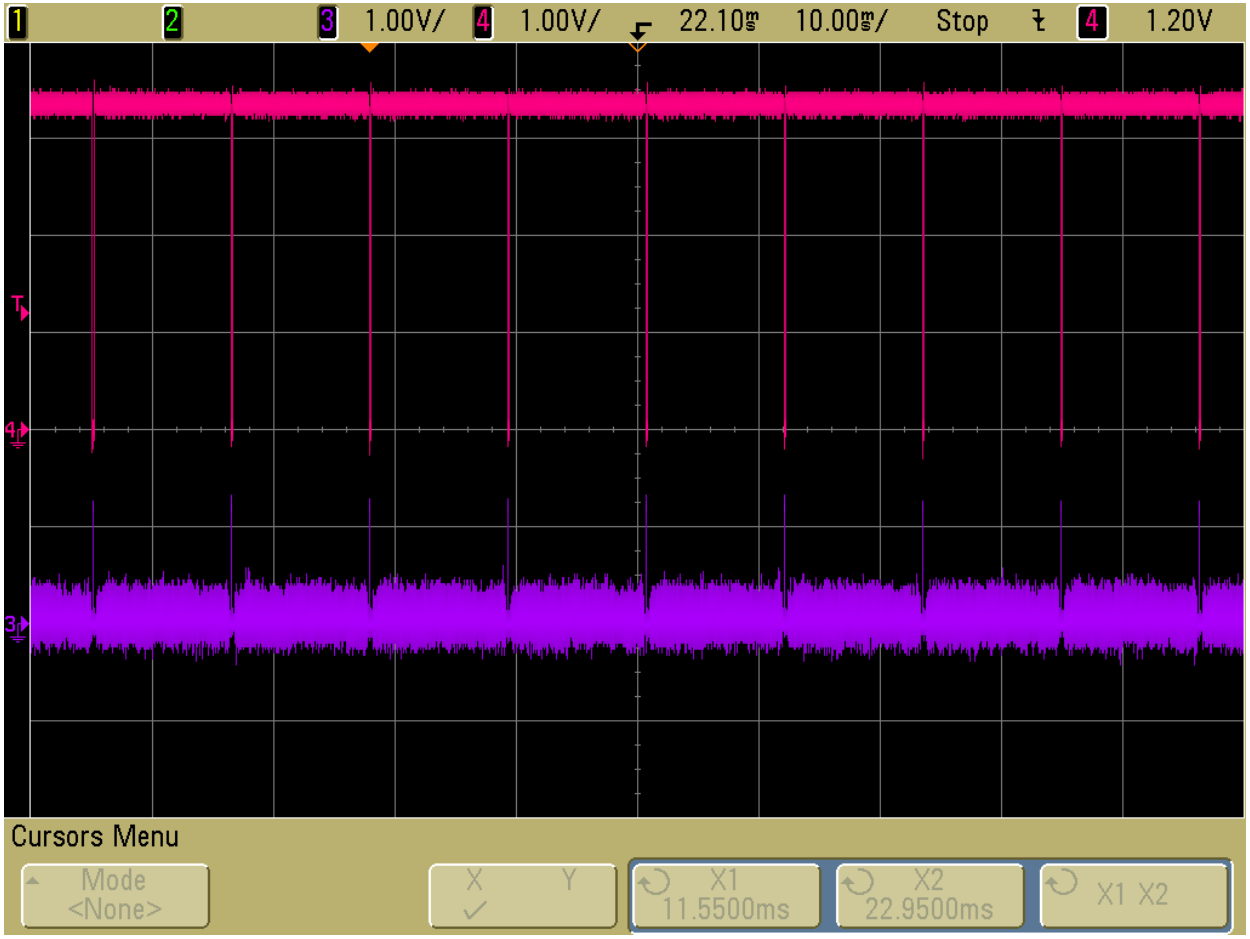
3A HS mode MIPI connection

- If there is MIPI connection with Rx
  - HS mode has about 300mV peak to peak waveform, please check every lane



3B Video mode output

- Blinking period (LP mode period) must be sync. with VSYNC

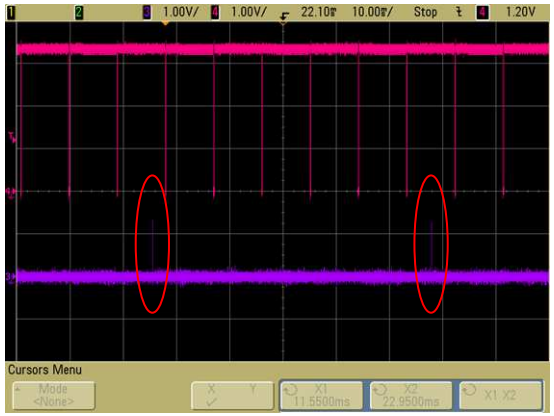


4A Q & A

Q: No display, MIPI video cannot sync with VSYNC

A: There is no display if porch setting or display size or polarity is wrong, check the following:

1. H/V Back Porch setting
2. HSYNC / VSYNC pulse width
3. PCLK / HSYNC / VSYNC polarity



4B Q & A

Q: No display, PLL > 600Mbps per lane

A: SSD2828 cannot support PLL > 600Mbps per lane. Also the maximum speed is limited by the MIPI connection between Tx and Rx, e.g. FPC connection and socket.

4C Q & A

Q: No display, even 0x11 and 0x29 are sent

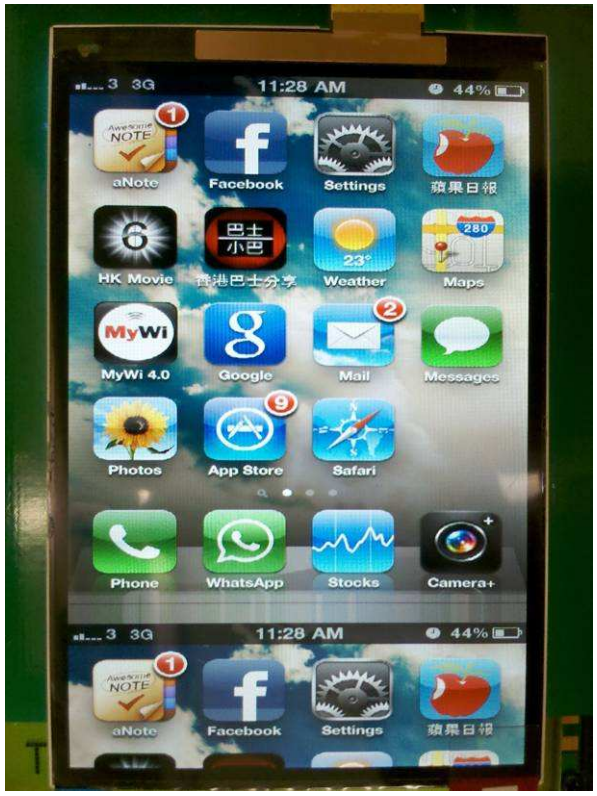
A: Several MIPI Rx ICs do not have internal oscillator, so they need MIPI clock for normal operation including generic/DCS command.

0xB7 bit 1 “CKE” must be “1” to enable HS clock output all the time.

4D Q & A

Q: End of the display has tearing effect

A: Pixel clock is too fast or PLL is too slow will cause such tearing effect.



Tearing effect

4E Q & A

Q: Display has red / blue / green dots

A: Noise from PCLK / HSYNC / VSYNC. Please reduce the noise or adjust delay time for PCLK.

red / blue / green dots

4F Q & A

Q: Display Shift

A: Wrong VSYNC/HSYNC setting. Check VSYNC/HSYNC width, polarity and porch settings.

5A AP SYNC and RGB check

1. Connect SCK, SDI and CS from TS5000